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H1K

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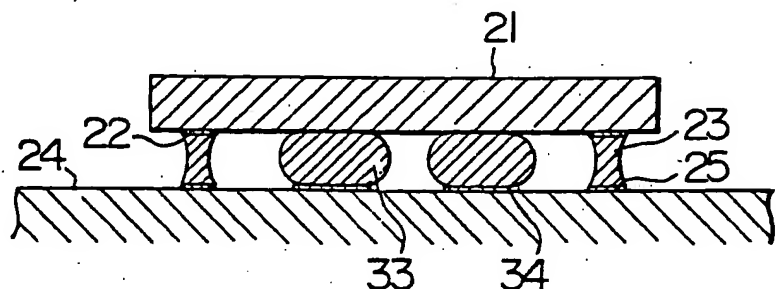
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(54) Semiconductor chip mountings

(57) A semiconductor chip with its
electrodes 22 connected to correspond-

ing electrodes 25 on a circuit board 24 by solder columns 23 is supported by solder spacers 33 formed on isolated metallised pads 34 on the circuit board, the spacers not wetting the chip. The arrangement is produced by forming solder bumps on the electrodes of the chip and circuit board and applying to the isolated pads layers of a solder of higher melting point and of a thickness less than the combined heights of the solder bumps. The chip is positioned on the circuit board with the solder bumps in contact and the temperature raised. The solder bumps melt and merge to form the columns 23 and the spacers then melt, surface tension causing the chip to be lifted so that the solder columns 23 are drawn into a cylindrical or hour-glass shape. Since the spacers do not wet the surface of the chip no lateral or rotational forces which might displace the chip are generated.

FIG.6



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FIG. 1
PRIOR ART

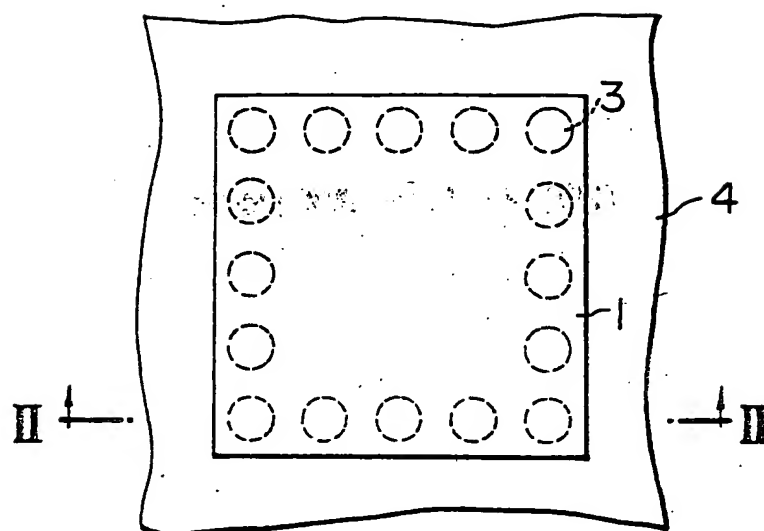


FIG. 2
PRIOR ART

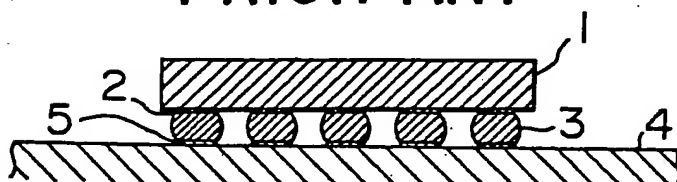


FIG. 3a
PRIOR ART

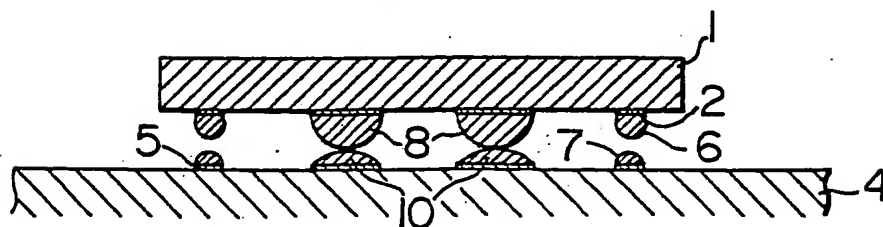
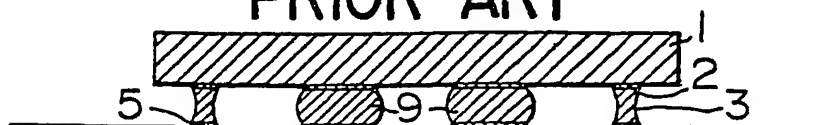


FIG. 3b
PRIOR ART



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FIG. 4a
PRIOR ART

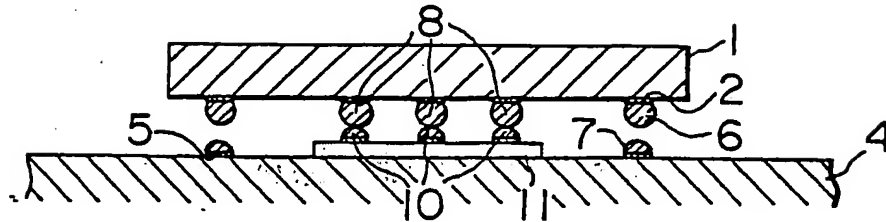


FIG. 4b
PRIOR ART

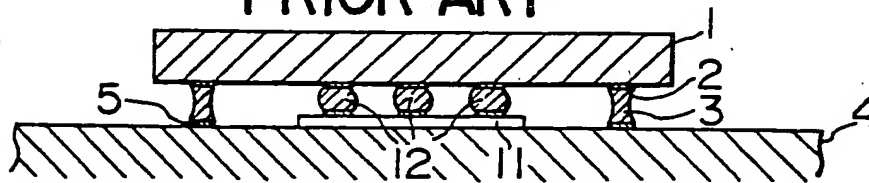
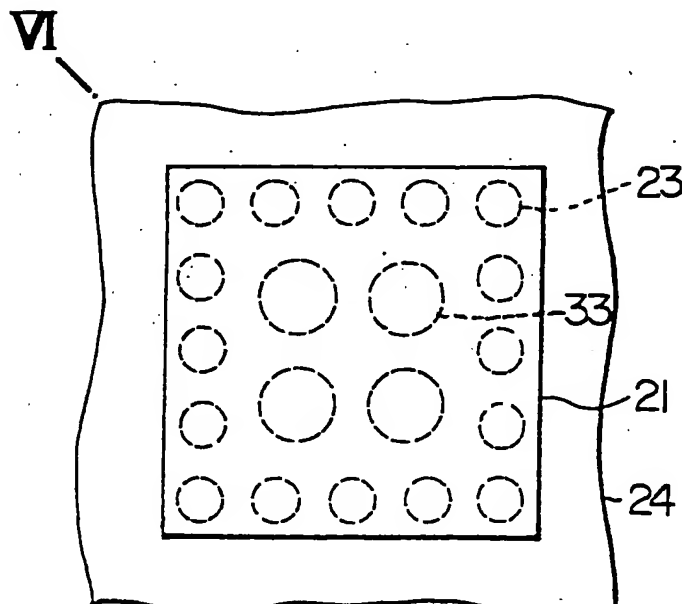


FIG. 5



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FIG. 6

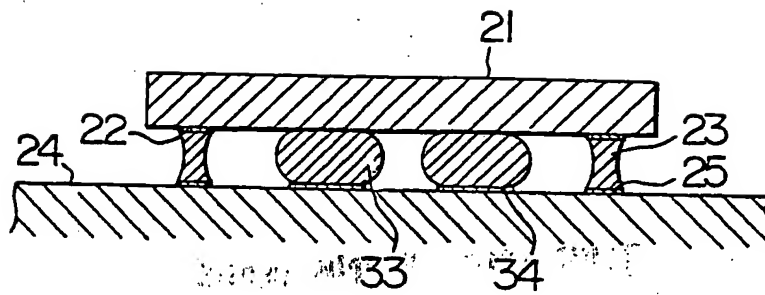


FIG. 7a

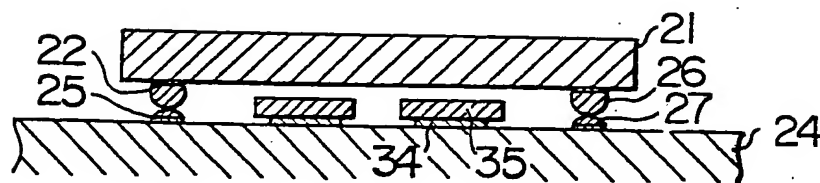


FIG. 7b

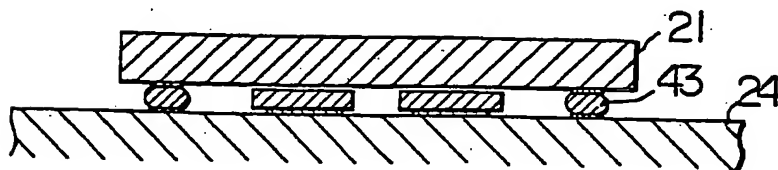
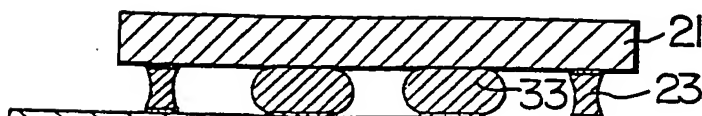


FIG. 7c



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SPECIFICATION

Semiconductor chip mounted structure and method of making the same

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The present invention relates to a semiconductor chip mounted structure in which a semiconductor chip including therein semiconductor devices is mounted on and bonded to a circuit board having an insulating substrate.

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There has been hitherto used a semiconductor chip mounted structure in which a semiconductor chip and electrodes on a circuit board are soldered through the face down bonding method, without using any lead wire therebetween, to mount the semiconductor chip on the board. A plan view and a sectional view of such a structure are as shown in Figures 1 and 2 of the accompanying drawings, respectively. The sectional view of Figure 2 is taken along line II-II in Figure 1. Referring to Figures 1 and 2, a semiconductor chip 1 is provided thereon with electrodes 2, and a circuit board 4 is provided thereon with electrodes 5 at positions substantially corresponding to those of the electrodes 2. The semiconductor chip 1 and the circuit board 4 are so positioned by known positioning means that each of the electrodes 2 is opposed to the corresponding one of the electrodes 5. Then, the chip 1 is connected and bonded to the circuit board 4 at some joining points, which are simultaneously soldered in such a manner as forming solder columns 3 by appropriate heating means such as a heating furnace, a soldering bath or the like.

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The above-mentioned chip mounted structure has an advantage that the time necessary for the bonding operation is not changed, even through the number of joining points were larger. In this structure, however, the semiconductor chip is bonded to the circuit board by means of solder, which is considerably deformable, without other intervening members. Accordingly, each of the joining points suffers from a thermal stress which is caused by generation of heat in the semiconductor chip, changes in the ambient temperature, and others, the strength of the thermal stress depending upon a difference in the thermal expansion coefficient between the semiconductor chip and the circuit board. Thus, the solder is disadvantageously fatigued and is apt to be separated from the electrodes on the circuit board. For the above reason, the environment in which the structure is employed, and the size of the semiconductor chip are restricted. This advantage stems from the fact that each of the solder columns 3 has a form of a spherical segment

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because the semiconductor chip is joined with the circuit board by the use of the natural melting and solidification of the solder forming the columns 3, and that each solder column therefore suffers from a concentrated stress at the interface between the solder column and the corresponding one of the electrodes on the circuit board when applied with an external stress. Further, in many cases, the interface between the solder column and the electrode becomes fragile due to reaction and/or diffusion which

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column and atoms forming the electrode. There has been known a structure which can solve the above-mentioned problem, and in which each of the solder columns 3 has a form of a circular cylinder or a sand-glass to distribute the external stress uniformly along the solder column and to make full use of the deformability of the solder column. (See, for example, U.S. Patent 3811186 issued on May 21, 1974.) In the above-mentioned structure, as shown in Figures 3a and 3b, there are provided between a semiconductor chip 1 and a circuit board 4 spacers 9 which are made of solder and used only for the mechanical connection between the chip 1 and the board 4, that is, used only to ensure the spacing between the chip 1 and the board 4. Further, electrodes 2 on the semiconductor chip 1 are connected to electrodes 5 on the circuit board 4 by solder columns 3, each of which has a form of a circular cylinder or a sandglass, depending upon the amount of solder for forming the each column 3.

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Further, there has been known such a structure as shown in Figures 4a and 4b, in which a dielectric plate 11 for supporting solder spacers 12 is provided on a circuit board 4, and each of solder columns 3 for electrically connecting electrodes 2 on a semiconductor chip 1 to electrodes 5 on the circuit board 4 is controlled by the spacers 12 so as to have a form of a circular cylinder or a sandglass.

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The inventors have found out that in these structures as shown in Figures 3a and 4a, when the semiconductor chip 1 and the circuit board 4 are positioned so that each of the electrodes 2 is opposed to the corresponding one of the electrodes 5, small solder mounds 8 on the semiconductor chip 1 make contact with small solder mounds 10 on the circuit board 4 or the dielectric plate 11 with small solder mounds 6 on the semiconductor chip 1 being spaced apart from small solder mounds 7 on the circuit board 4. This is because of the different amounts of solder for the small mounds 6, 7 and 8, 10 such that the connecting or bonding solder columns 3 finally take a form of a circular cylinder or a sandglass. The small mounds 6 are brought in contact with the small mounds 7 after the small mounds 8 and 10 have melted and reflowed so as to form spacers 9 or 12. Accordingly, the form of the bonding solder column 3 is variable depending upon the manner in which the small mounds 8 and 10 melt and solidify as well as upon variations in the height of the mounds 8 and 10. In the worst case, the solder column 3 is subjected to torsion, and false connection takes place. That is, in the two structures shown in Figures 3a, 3b, 4a and 4b, it is very difficult to obtain the solder columns 3 having an optimum form. Further, in the structure shown in Figures 4a and 4b, it is required to form the dielectric plate 11 with a high accuracy.

An object of the present invention is to provide a semiconductor chip mounted structure, in which the form of a solder column for connecting or bonding a semiconductor chip to a circuit board can be readily controlled free from the drawbacks of the conventional structures.

Another object of the present invention is to

which a semiconductor chip and a circuit board are soldered at all joining points with higher reliability free from the drawbacks of the conventional structures.

- 5 A further object of the present invention is to provide a method of making a semiconductor chip mounted structure, in which a semiconductor chip and a circuit board are soldered at all joining points with a high work efficiency free from the drawbacks of the conventional methods.

10 According to the present invention which attains these and other objects, there are provided a semiconductor chip mounted structure and a method of making such a structure: in which
15 isolated metallized pads are provided on a circuit board along with solder thereon assuming the state of a sheet or paste; and in which by heating the structure the semiconductor chip and the circuit board are first soldered at electrode portions to be
20 connected or bonded and then the solder on the isolated metallized pads melts, so that the molten solder on the isolated pads pushes up the semiconductor chip on the basis of the surface tension of the molten solder without wetting the semiconductor
25 chip, whereby the molten solder at each connecting electrode portion has a form of a circular cylinder or a sandglass, and then both the molten solder on the isolated pads and the molten solder at the connecting electrode portions are set or solidified.

30 In more detail, in the above-mentioned structure, since solder pillars finally formed on the circuit board do not wet the semiconductor chip, the semiconductor chip is pushed up by the pillars without being moved in a horizontal direction and
35 without being rotated in a horizontal plane, and therefore the connecting or bonding solder for electrically connecting the semiconductor chip and the circuit board is not subjected to torsion but has a controlled form of a circular cylinder or a sandglass.

40 Further, since the thickness of solder supplied in the state of a sheet or paste and placed on the isolated metallized pads is small as compared with the spacing between the semiconductor chip and the circuit board when the semiconductor chip and the
45 circuit board are positioned so that the semiconductor chip is kept in contact with the board through the solder at the connecting electrode portions, satisfactory soldering can be ensured at the connecting electrode portions when heating temperature is
50 raised. Furthermore, the form and the height of the solder at the connecting electrode portions can be readily controlled by changing the ratio of the volume of the solder placed on the isolated metallized pad to the area of the isolated pad.

- 55 In the accompanying drawings:

Figure 1 is a plan view showing connecting portions of a semiconductor chip mounted structure through the conventional face down bonding method;

60 *Figure 2* is a sectional view of the connecting portions, taken along the line II-II in *Figure 1*;

Figure 3a is a sectional view showing connecting portions of a semiconductor chip structure, in which solder spacers are provided between a circuit board

been effected between the board and the semiconductor chip for connection through the conventional face down bonding method;

Figure 3b is a sectional view of the structure of
70 *Figure 3a* as finally bonded, in which the semiconductor chip has been connected and bonded to the circuit board;

Figure 4a is a sectional view showing connecting portions of a semiconductor chip mounted structure,
75 in which solder spacers are provided on a dielectric plate and the positioning has been effected between a semiconductor chip and a circuit board for connection through the conventional face down bonding method;

80 *Figure 4b* is a sectional view of the structure shown of *Figure 4a* as finally bonded, in which the semiconductor chip has been connected and bonded to the circuit board;

Figure 5 is a plan view showing connecting portions of a semiconductor chip mounted structure in accordance with the present invention;

Figure 6 is a sectional view of the connecting portions, taken along the line VI-VI in *Figure 5*; and

Figures 7a, 7b and 7c are sectional views for
90 explaining various steps of a process for bonding a semiconductor chip to a circuit board in accordance with the present invention.

Now, explanation will be made on an embodiment of the present invention with reference to the
95 accompanying drawings.

In *Figure 5* showing in plan view connecting portions of a semiconductor chip mounted structure in accordance with the present invention, solder columns 23 for electrically connecting or bonding a
100 semiconductor chip 21 and a circuit board 24 are arranged at many positions on a peripheral part of the semiconductor chip 21, and solder spacers 33 are placed on the circuit board 24 at positions corresponding to a central part of the semiconductor chip
105 21. *Figure 6* is a sectional view of the connecting portions, taken along the line VI-VI in *Figure 5*. Referring to *Figure 6*, the semiconductor chip 21 is electrically connected to the circuit board 24 by the bonding solder columns 23 in such a manner that
110 the height and the form of the bonding solder columns 23 are controlled by the solder spacers 33 provided on isolated metallized pads 34 formed on the circuit board 24.

Next, a process of making the structure shown in
115 *Figures 5 and 6* will be explained with reference to *Figure 7a, 7b and 7c*. First, solder is deposited on electrodes 22, which have been provided on a semiconductor chip 21 such as an integrated circuit, at predetermined positions through evaporation techniques or the like. The solder thus deposited
120 is melted and then solidified by appropriate heating means to form small solder mounds 26 having a diameter of about 150 μm and a height of about 80 to 120 μm . In this case, a solder containing lead as the main component and 5 to 10 weight % of tin is employed. However, another solder having a lower melting point may be employed.

On the other hand, conductive paste (for example, a conductive Ag-Pd paste) is printed on a circuit

electrodes 2 and at other positions on the semiconductor chip 21, and then fired to form electrodes 25 corresponding to the electrodes 22 and to form isolated metallized pads 34. Next, solder is supplied
 5 onto the pads 25 by printing solder paste on the pads 25. The solder is then melted and solidified to form on each of the pads 25 a small solder mound 27 having a diameter of about 150 to 200 μm and a height of about 30 to 50 μm . The solder for the
 10 mounds 27 may be one having the same composition as that used to form the small mounds 26. Further, solder 35 which may be a sheet about 80 to 150 μm thick or a printed film of paste having a thickness of about 80 to 150 μm , is placed on each of
 15 the isolated pads 34, and temporarily fixed to each isolated pad 34 by a flux applied thereto. The material for the solder 35 is so selected as to be higher in melting point than the solder for the small mounds 6 and 7 by about 5 to 6°C. Then, the
 20 positioning is effected between the semiconductor chip 21 and the circuit board 24, which have been subjected to the above-mentioned treatment, using appropriate positioning means, and the semiconductor chip 21 is temporarily fixed to the board 24 by
 25 a flux applied to the small solder mounds 27. Thus, there is formed such a structure as shown in Figure 7a. Next, the structure shown in Figure 7a is heated to a temperature which is higher than the melting point of the solder 35 by about 20°C or more, by
 30 appropriate heating means such as a heating furnace or a soldering bath. When the temperature of the structure shown in Figure 7a is raised, the small solder mounds 26 and 27 first melt, and form bonding solder columns 43 for connecting the
 35 semiconductor chip 21 and the board 24, as shown in Figure 7b. That is, the chip 21 is connected or bonded to the board 24 by the bonding columns 43 made of molten solder. Then, the solder 35 melts, and forms on the isolated pads 34 solder spacers 33
 40 each made of molten solder and having the form of a pillar. The semiconductor chip 21 is pushed up by the solder spacers 33 without being moved in a horizontal direction and without being rotated in a horizontal plane, because the solder spacers 33 don't
 45 wet the semiconductor chip 21. Thus, each of the solder columns 43 is elongated so as to have a form of a circular cylinder or a sandglass 23, as shown in Figure 7c. The structure shown in Figure 7c is then cooled to room temperature, and thus the semiconductor chip 21 is bonded to the circuit board 24. That
 50 is, electrical and bonding between the chip 21 and the board 24 is completed.

Further, the moment of the gravity applied to the center of gravity of the semiconductor chip 21 with
 55 respect to the geometrical center of the semiconductor chip 21 depends upon the weight distribution of wiring conductors provided on the semiconductor chip 21, the weight distribution of the bonding solder columns 23, and the weight distribution of the semiconductor chip 21 itself. In order for the
 60 surface tension of the molten solder 33 formed on the isolated pads 34 to withstand the above-mentioned moment of the gravity, and to space the semiconductor chip 21 part from the circuit board 24

are to be arranged at the outside of the electrodes 25, if possible, though such an arrangement is not shown in the accompanying drawings.

As has been explained hereinbefore, according to
 70 the present invention, solder spacers only for pushing up a semiconductor chip are formed on isolated metallized pads provided on a circuit board, and each of solder columns for connecting or bonding the semiconductor chip and the circuit
 75 board is elongated by the surface tension of the solder spacers so as to have the form of a circular cylinder or a sandglass. That is, the solder columns having a desired shape can be readily formed, and moreover the stress applied to each solder column is
 80 distributed uniformly along the axis of the solder column. Thus, the semiconductor chip is connected or bonded to the circuit board with high reliability. Further, the solder spacers serve as lead for radiating heat generated in the semiconductor chip,
 85 thereby further increasing the reliability of the structure. The semiconductor chip mounted structure in accordance with the present invention has such various advantages as mentioned above, and therefore can make a great contribution to a technical
 90 field including hybrid integrated circuits which will be employed more widely.

CLAIMS

95 1. A semiconductor chip mounted structure comprising:

- (a) a semiconductor chip having on a surface thereof at least one electrode for external connection;
- 100 (b) a circuit board having on a surface thereof at least one electrode for external connection and at least one isolated metallized pad, said electrode for external connection being provided at a position opposite to said electrode for external connection provided on said semiconductor chip, said isolated pad being provided at a position shifted from said electrode for external connection provided on said semiconductor chip;
- 105 (c) at least one bonding column made of solder and having a form of a circular cylinder or a sandglass, said bonding column being provided between said electrode for external connection provided on said semiconductor chip and said electrode for external connection provided on said circuit board, said electrode for external connection provided on said semiconductor chip being opposed to said electrode for external connection provided on said circuit board; and
- 115 (d) at least one spacer made of solder and provided on said isolated pad, said spacer keeping said semiconductor chip spaced apart from said circuit board without wetting said semiconductor chip, said spacer being higher in melting point than said connecting column, said spacer having the form
 125 of a pillar.

2. A structure according to Claim 1, wherein a plurality of isolated pads are provided and a plurality of bonding columns are provided, and wherein said isolated pads are arranged outside of said bonding

3. A method of making a semiconductor chip mounted structure comprising the steps of:

- 5 (a) forming small mounds of a predetermined amount of solder on a semiconductor chip provided with a connecting electrode and on a circuit board provided with a connecting electrode, said connecting electrodes being to be connected to each other;
- 10 (b) placing on an isolated metallized pad a layer of a predetermined amount of solder, said isolated pad being provided on said circuit board at a position shifted from the position of said connecting electrode, said solder for forming said layer being higher in melting point than said solder for forming said small mounds, said layer having a thickness smaller than the sum of respective height of said small mounds;
- 15 (c) effecting positioning between said semiconductor chip and said circuit board, and heating said semiconductor chip and said circuit board to a predetermined temperature, said semiconductor chip being provided with said connecting electrode and said small mound, said circuit board being provided with said connecting electrode, said small mound, said isolated electrode and said layer, said predetermined temperature being higher than the melting point of said solder for forming said layer; and
- 20 (d) cooling said semiconductor chip and said circuit board to another predetermined temperature lower than the melting point of said solder for forming said small mounds.
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4. A method according to Claim 3, wherein said

layer has a predetermined size, wherein said small mound made on said semiconductor chip is formed on said connecting electrode provided on said semiconductor chip, wherein said small mound made on said circuit board is formed on said connecting electrode provided on said circuit board, wherein said connecting electrodes are arranged so as to face other, and wherein said solder for forming said layer is higher in melting point than said solder for forming said small mound on said connecting electrode provided on said circuit board.

5. A method according to Claim 3, wherein when layer is heated to said predetermined temperature, said solder for forming said layer melts and the molten solder has the form of a pillar.

6. A method according to Claim 3, wherein said small mounds form a column having the form of a sandglass when heated to said predetermined temperature.

7. A method according to Claim 3, wherein when said layer is heated to said predetermined temperature, said solder for forming said layer melts and the molten solder pushes up said semiconductor chip to a predetermined height.

8. A semi-conductor chip mounted structure substantially as hereinbefore described with reference to and as shown by Figures 5 and 7 of the accompanying drawings.

9. A method of making a semiconductor chip mounted structure substantially as hereinbefore described with reference to Figures 5 to 7 of the accompanying drawings.